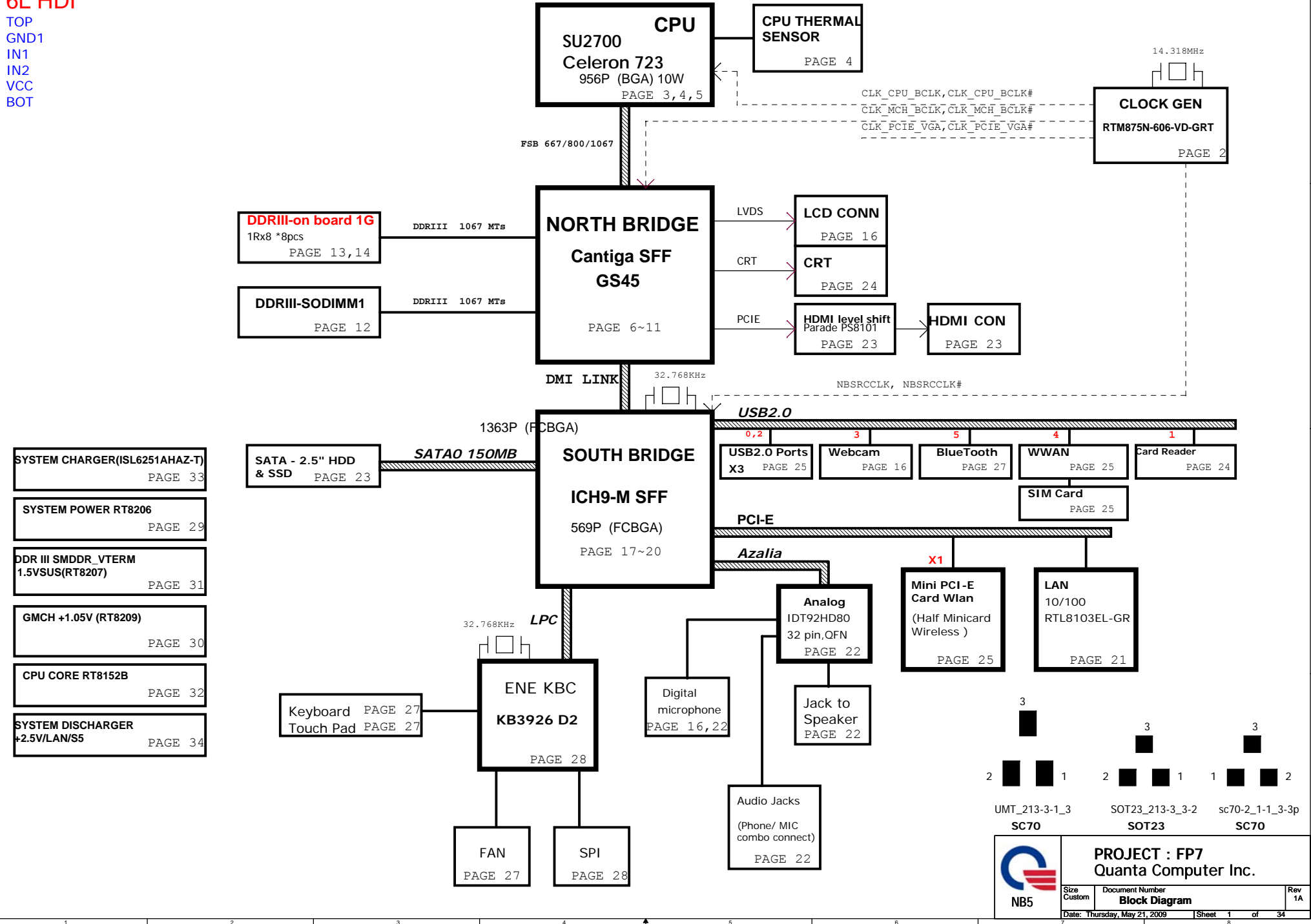


FP7 (CULV) BLOCK DIAGRAM

01

PCB STACK UP
6L HDI

TOP
GND1
IN1
IN2
VCC
BOT



5/13

5

4

3

2

1

1.Del Vcc_HDA R5234 (short0402)

2.C5533, C5541, C5205, C5291, R5233 嘲桔 BGA 條啾 ,叫 ㄟfoot print磊PAD 確 よ

3.op6v-0513 update net import 瓜,叫腊T ㄟ ン swap pin

4.PR158 net change from +5VSUS to +3VSUS.

5.PR182 net change from +10VALW to +15VALW.

6.NET NAME Change from R_CLK_VAG_OE# to R_CLK_WWAN_OE#.

7.NET NAME Change from CLK_VGA_OE# to CLK_WWAN_OE#.

8.New add R8 ,R9, R10 ⇐ CRT_R,CRT_G,CRT_B for EMI

5/14

1.New add C7362 C7366 C7357 C7378 C7379 C7367 for CRT RGB EMI

2.New add GND PAD Footprint SPAD-RE170x945

3.del T5007,T5037,T5039,T5044.

5/15

1.update power schematic for LV cup 絮潰.

5/18

1.update rename.

2.Del H7034,H7033.

3.C7354 and C7359 璫 ン.

4.NEW ADD KBC test PAD on GPXA and GPXD

5.Change footprint CN14,CN3,CN4,CN5,CN7,CN9,PL4,PL5,PL6

6.New add C557 for EMI.

7.R124 Footprint change to RC0402

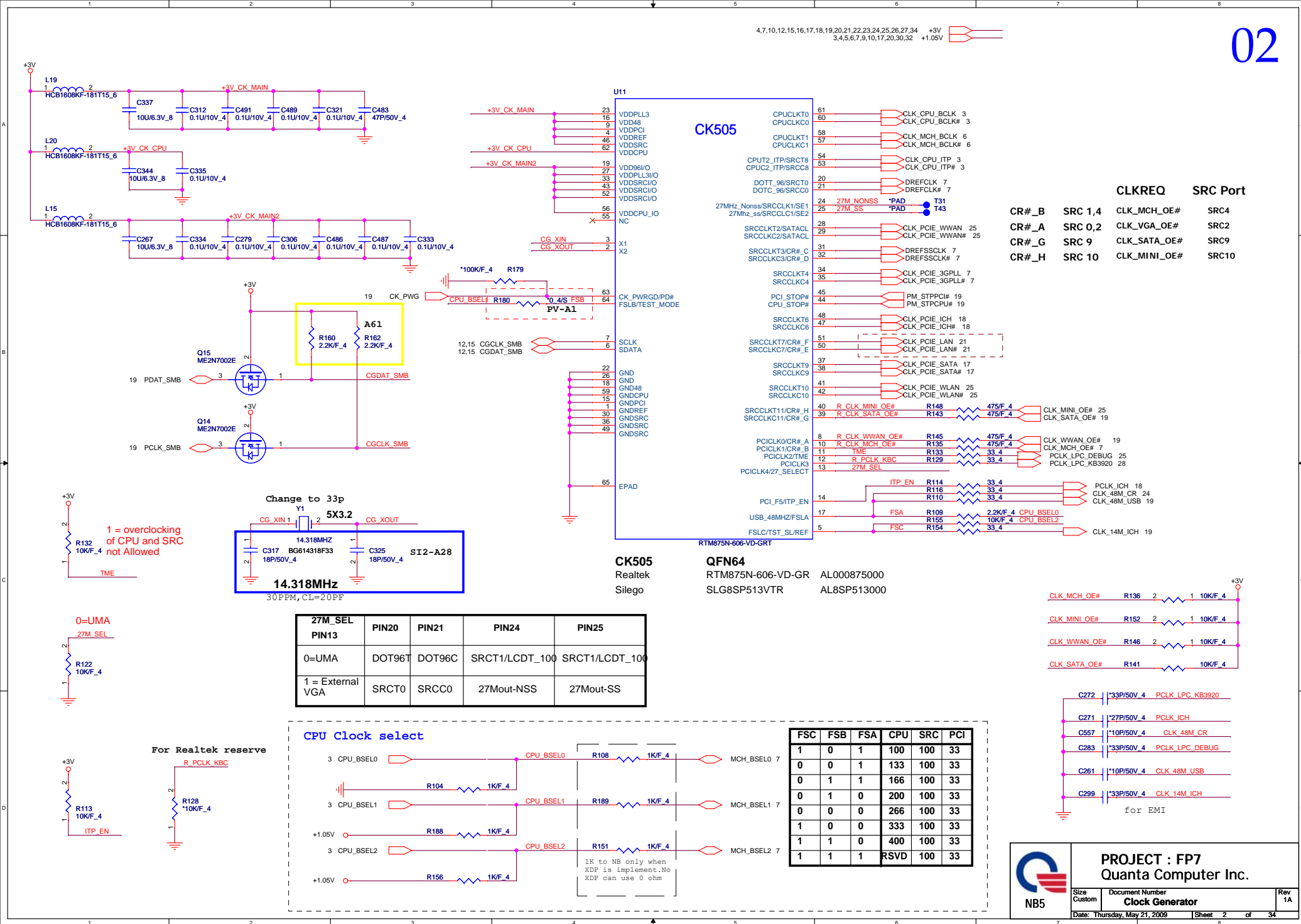
8.Change LAN from G to 10/100(传Transformer)

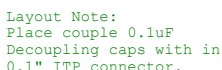
9.WWAN--->New add R368,R360,C512,C513,C522.

10.DEL NET-->MDI2+,MDI2-,MDI3+,MDI3-.

11.ADD R734,C534,R378,RC523 for HSYNCcmVSYNC.

Title			
<Title>			
Size	Document Number		Rev
A3	<Doc>		<RevCo
Date:	Thursday, May 21, 2009	Sheet 1 of 1	

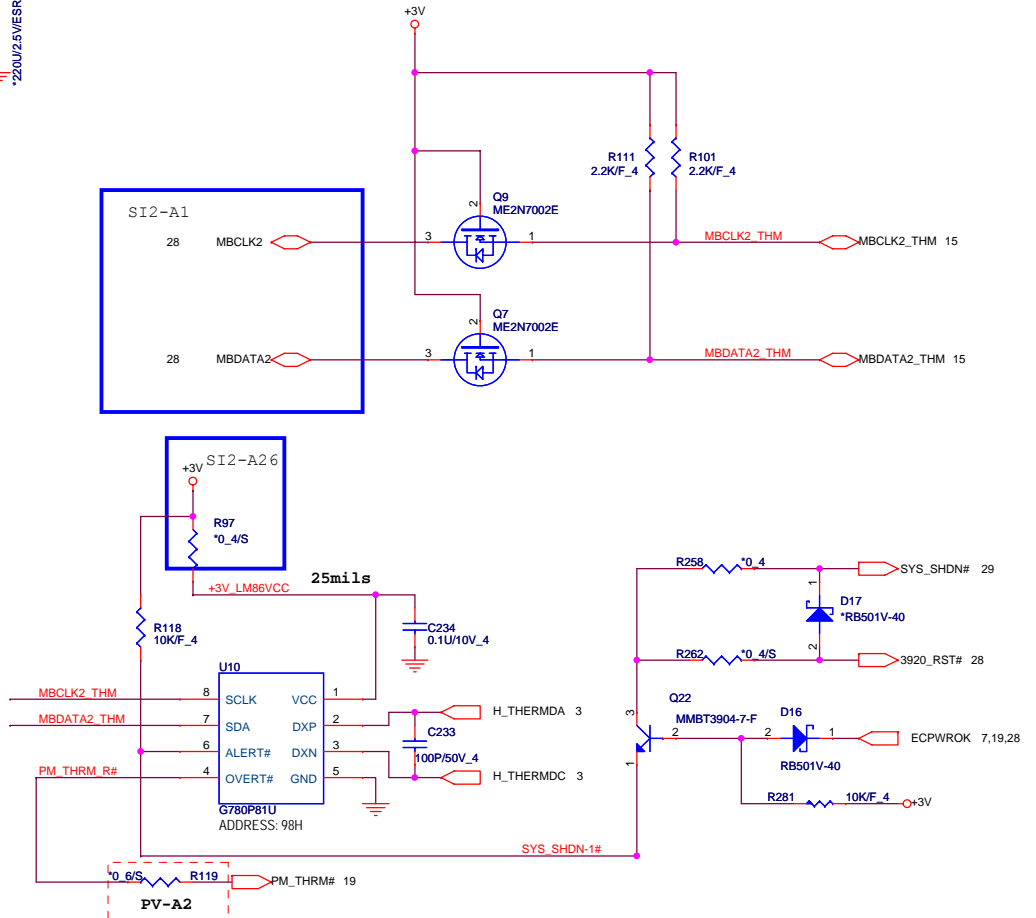
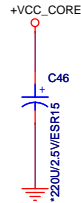


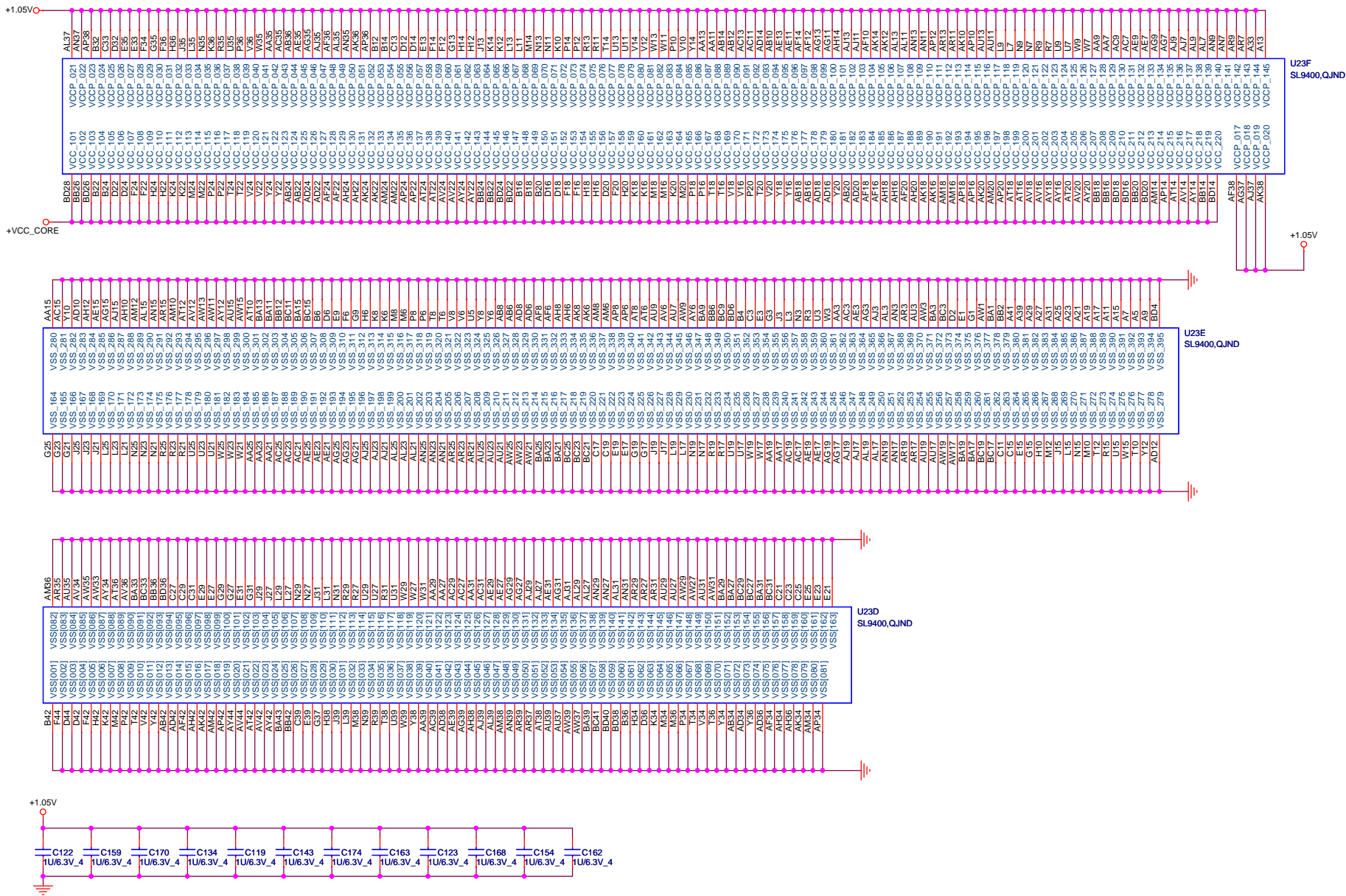


*PAD T14 CPU TEST3
*PAD T40 CPU TEST5
*PAD T37 CPU TEST6

For the purpose of testability, route these signal through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

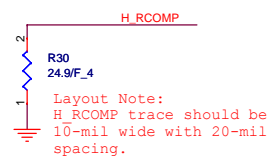
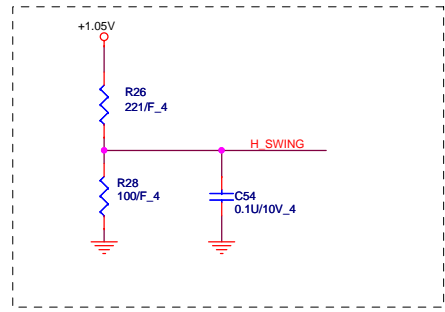




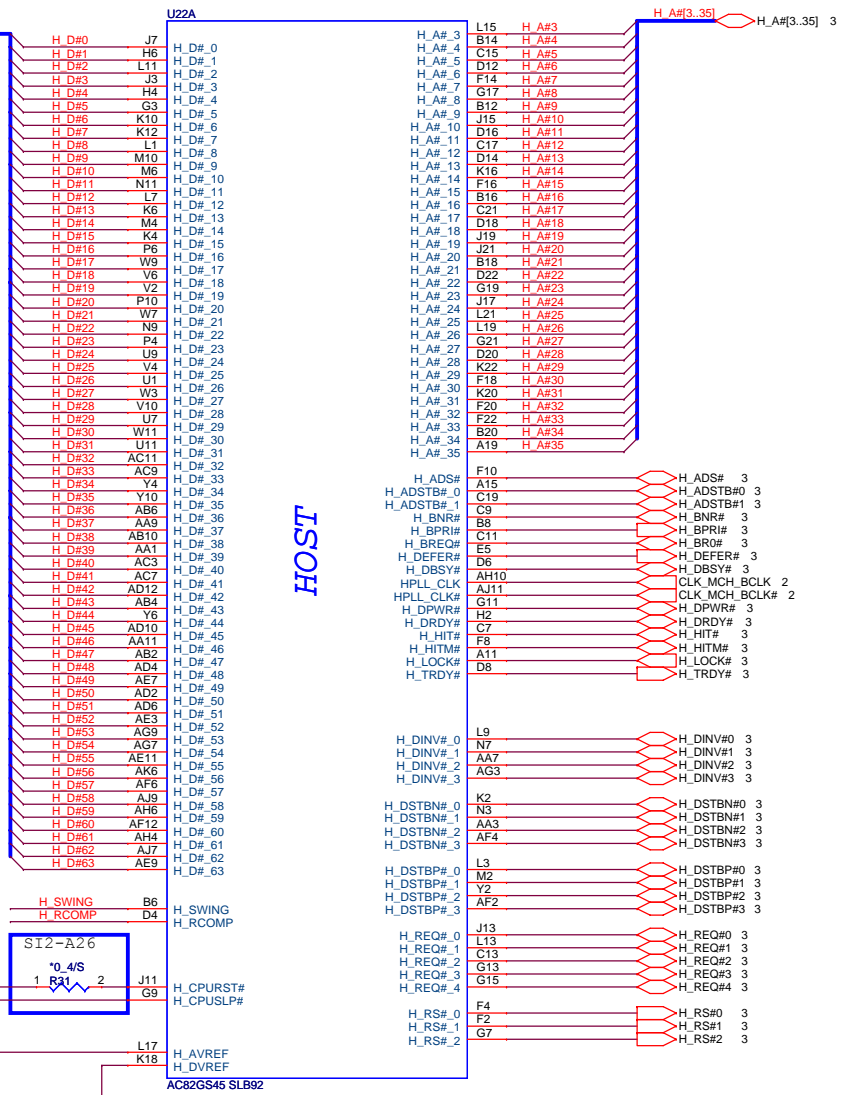
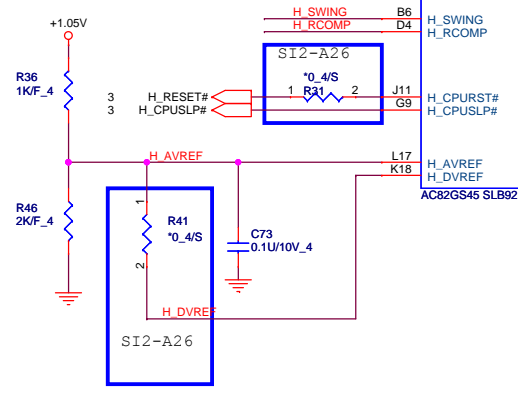


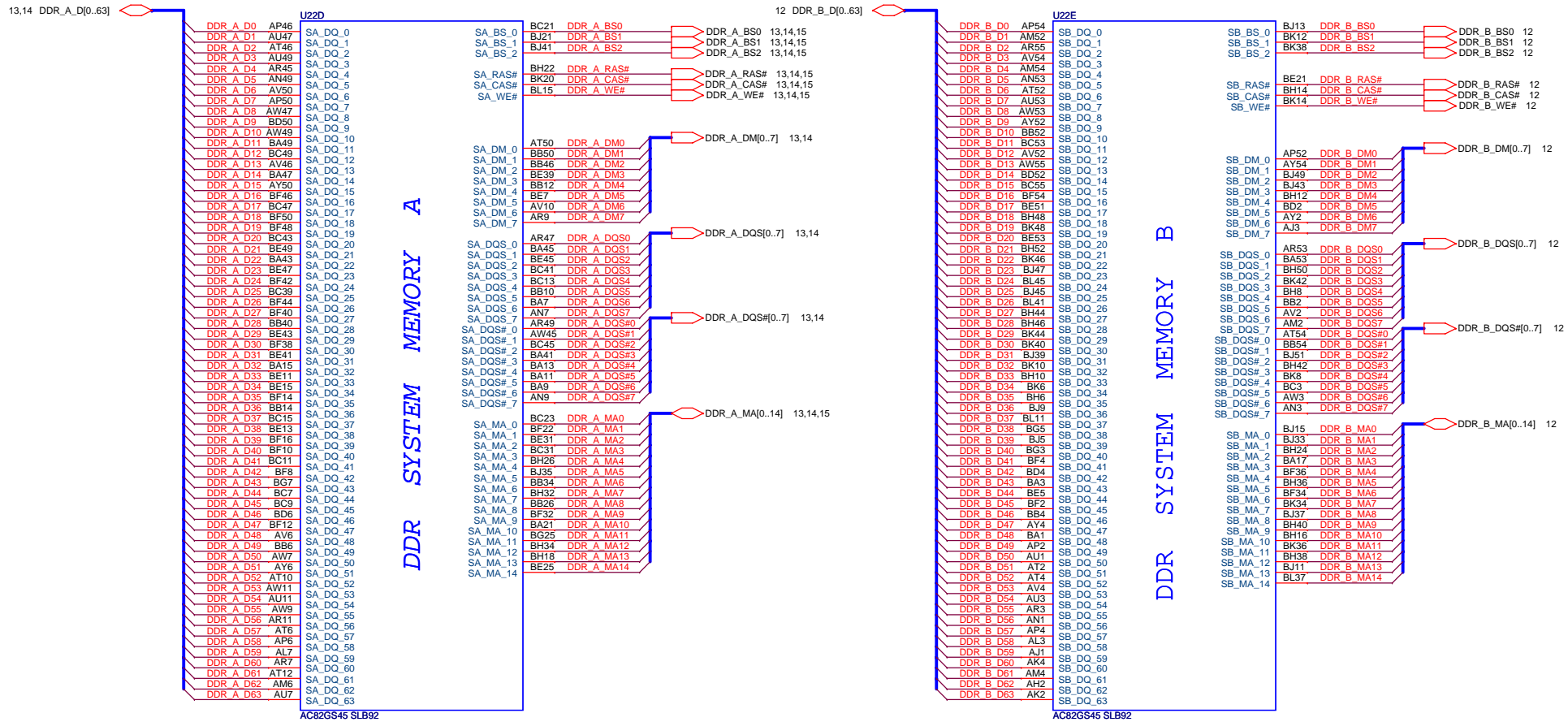
PROJECT : FP7
Quanta Computer Inc.


Size Custom	Document Number Penryn 3/3	Rev 1A
Date: Monday, May 25, 2009	Sheet 5 of 34	



Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



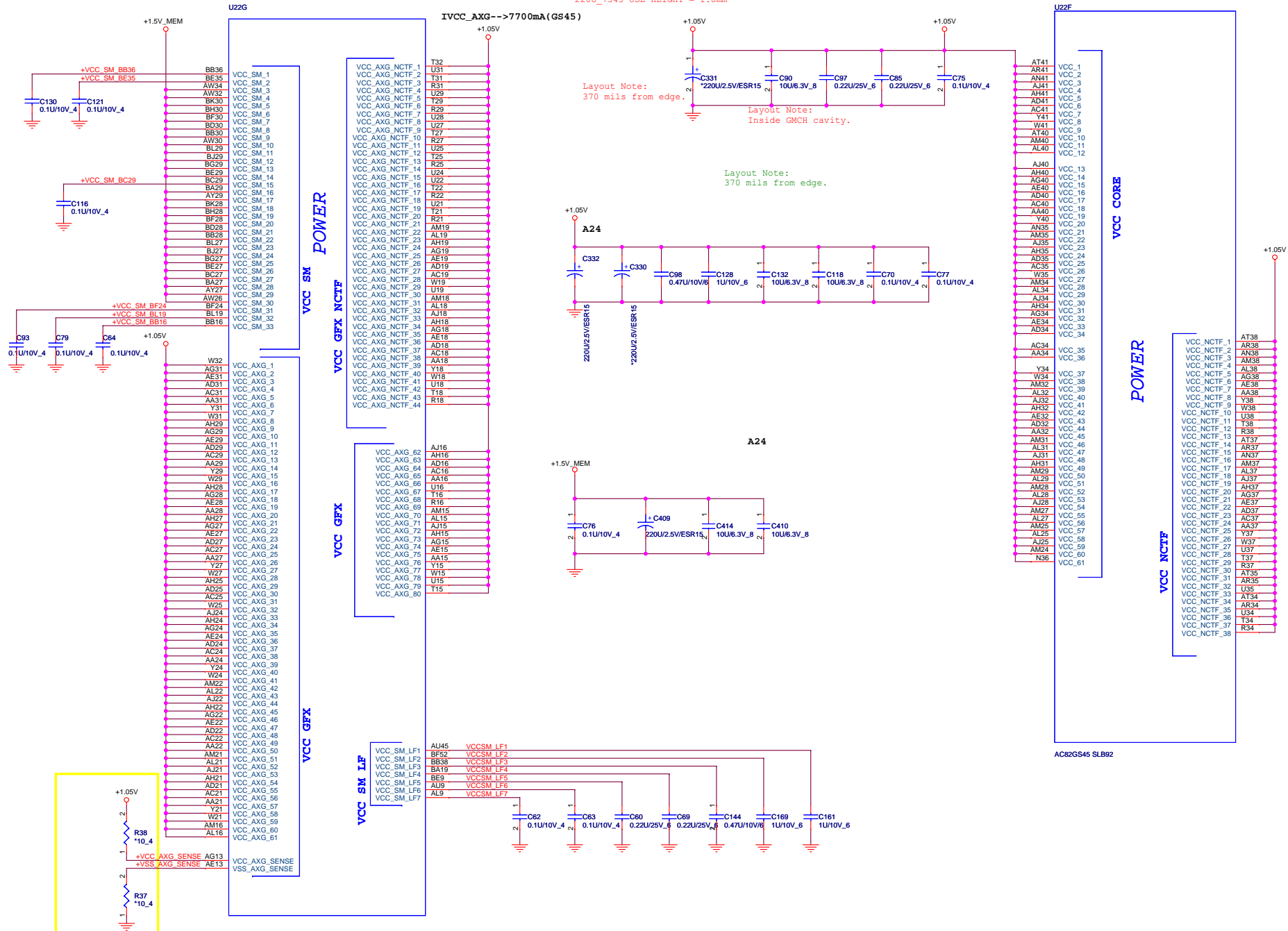


 NB5	PROJECT : FP7		
	Quanta Computer Inc.		
	Size Custom	Document Number Cantiga (DDR interface)	Rev 1A
Date: Thursday, May 21, 2009		Sheet 8 of 34	

Ivcc_sm (DDR3,1.5V,1066MTs) -->4140mA

220U_7343 USE HEIGHT = 1.8mm

IVCC_AXG-->7700mA(GS45)



PROJECT : FP7
Quanta Computer Inc.

Size Custom	Document Number Cantiga (Vcc)	Rev 1A
Date: Thursday, May 21, 2009	Sheet 9 of 34	



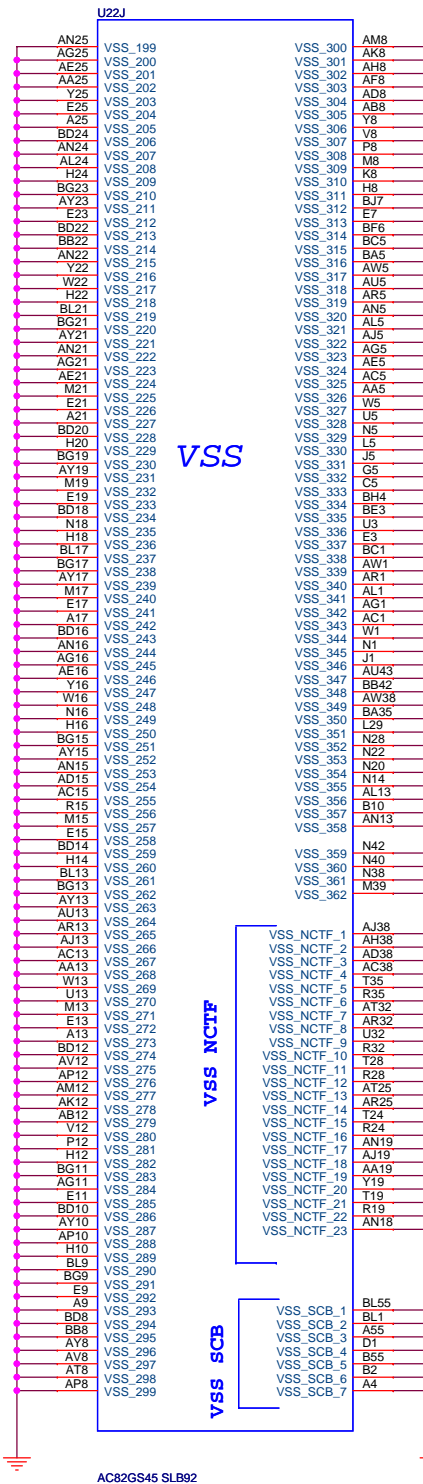
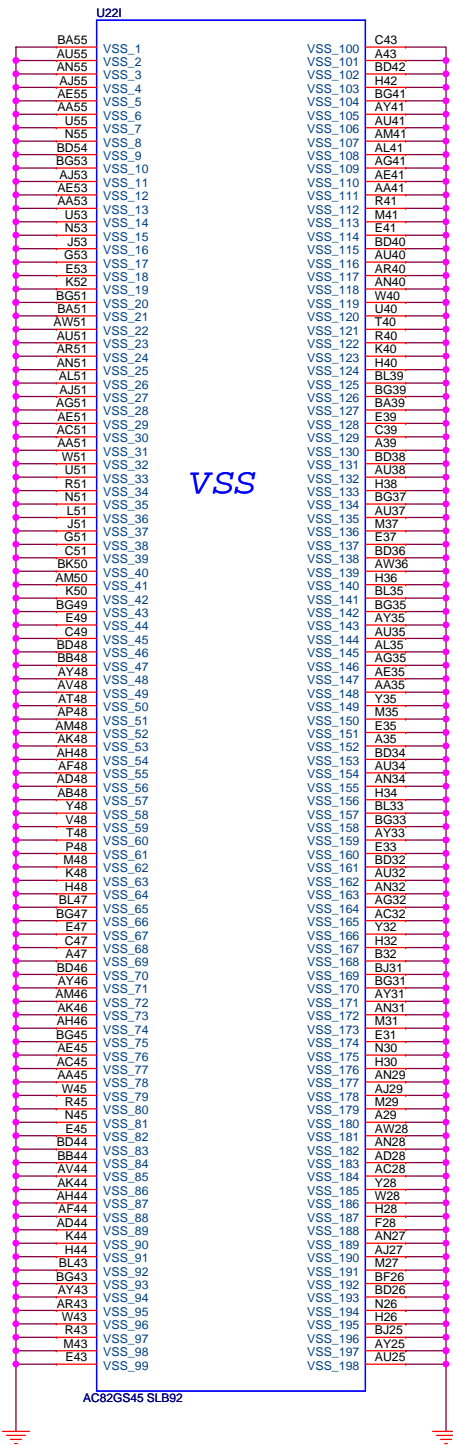
PROJECT : FP7
Quanta Computer Inc.

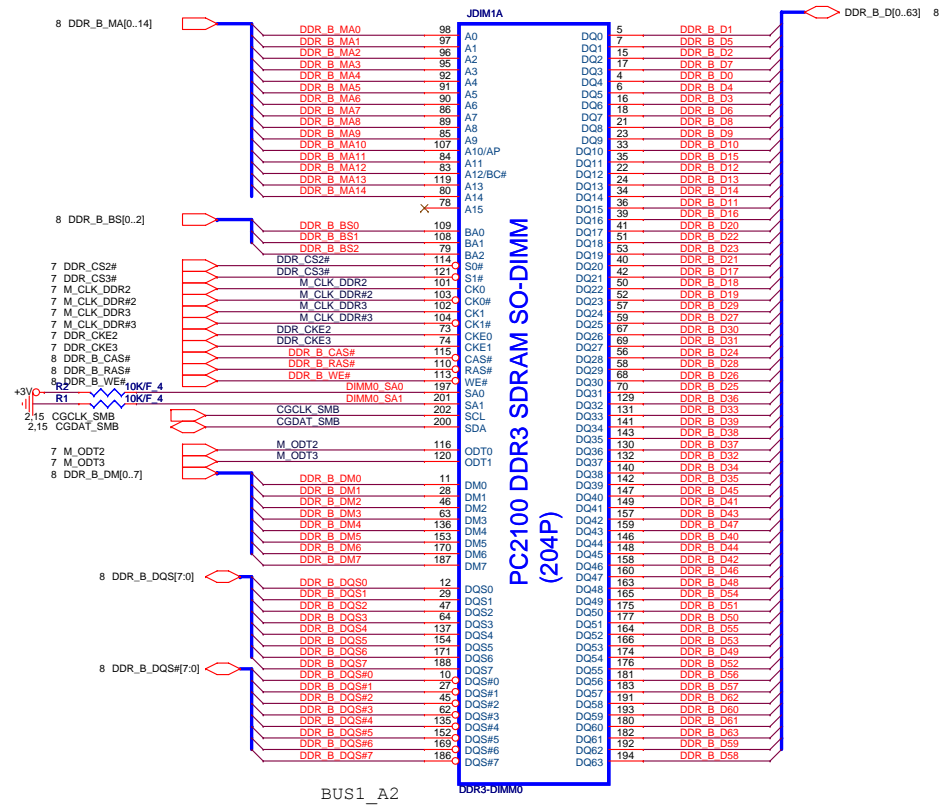
	Size Custom
--	-------------

Document Number
Cantiga (Power)

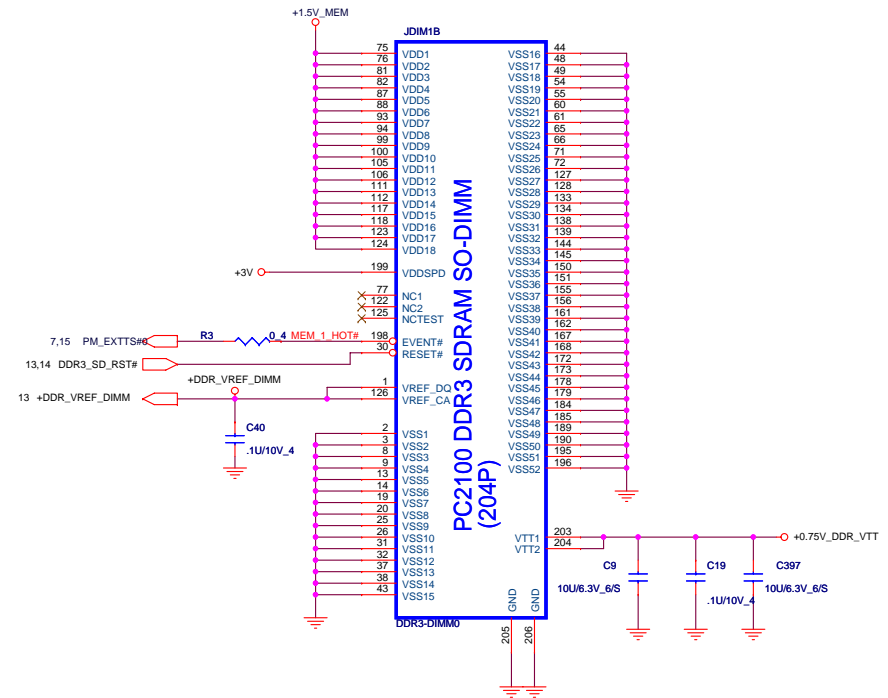
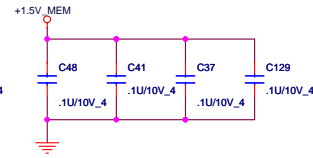
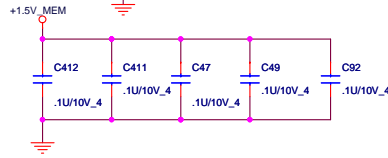
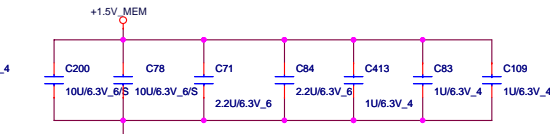
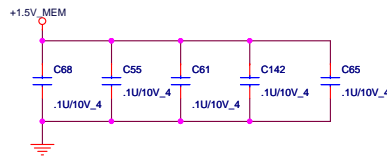
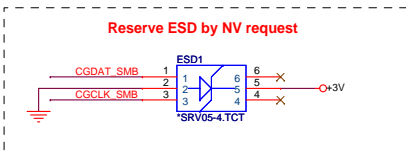
	Rev 1A
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Date: Thursday, May 21, 2009 Sheet 10 of 34





SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

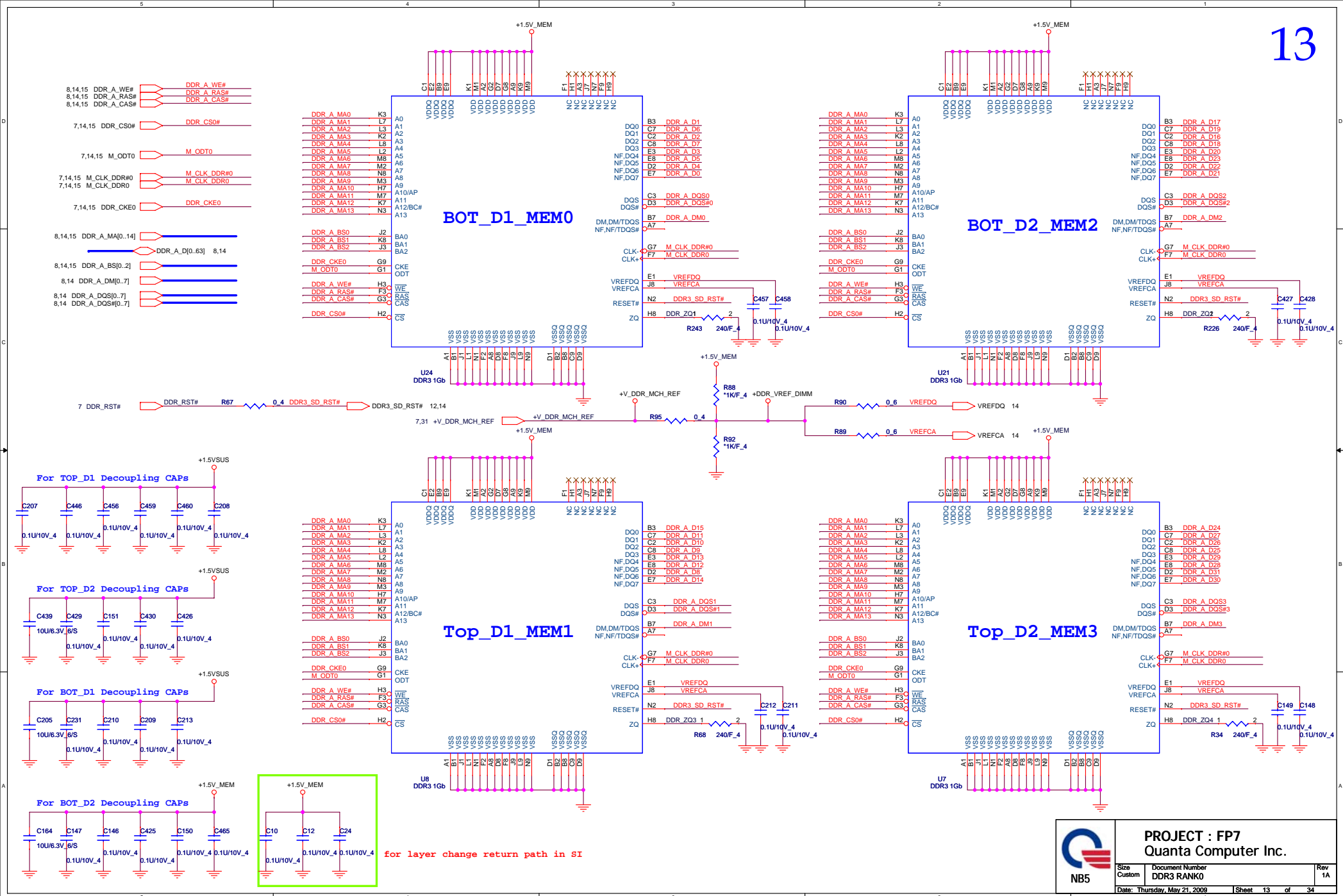


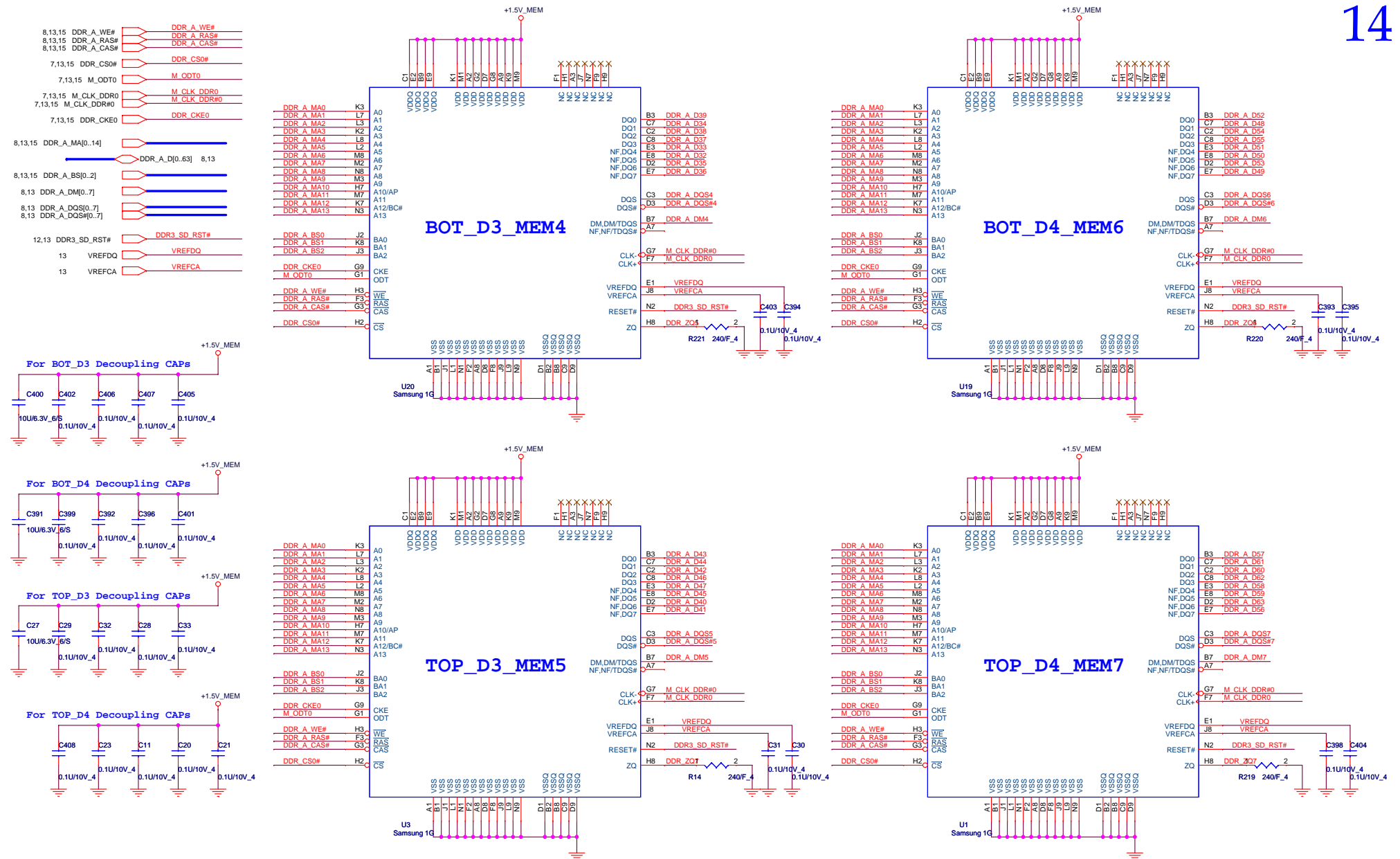
MEM delay circuit deleted by
DG-03328-001-V15

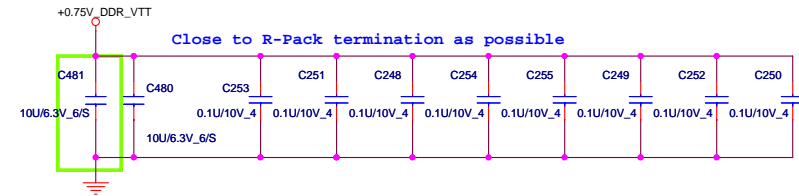
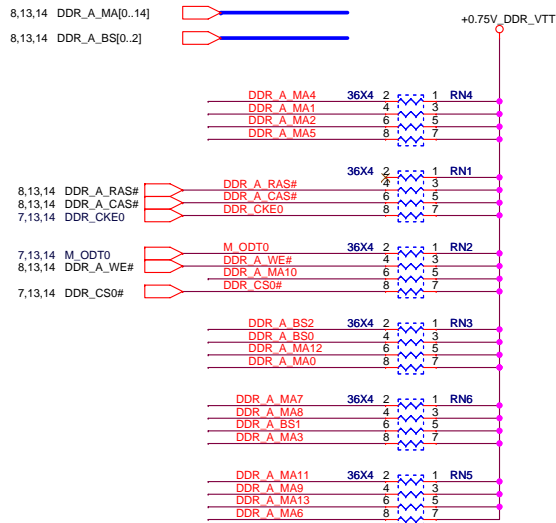


PROJECT : FP7
Quanta Computer Inc.

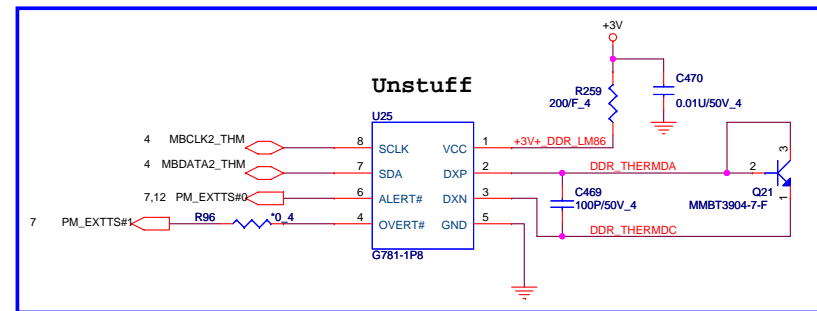
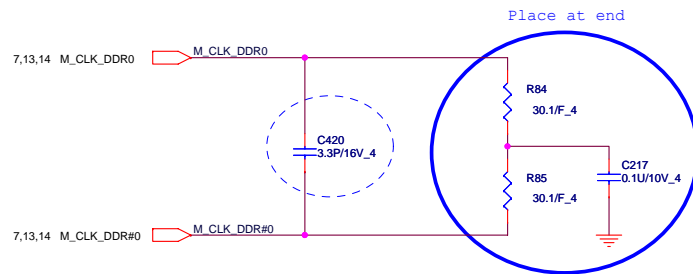
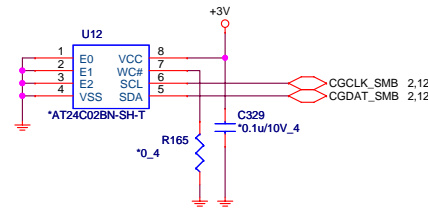
Size	Document Number	Rev
Custom	DDR3 SO-DIMM(200P)	1A
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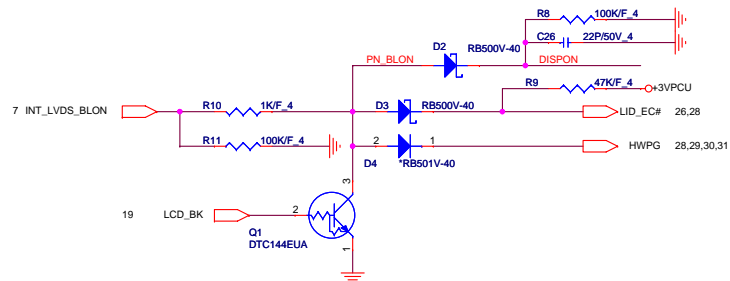




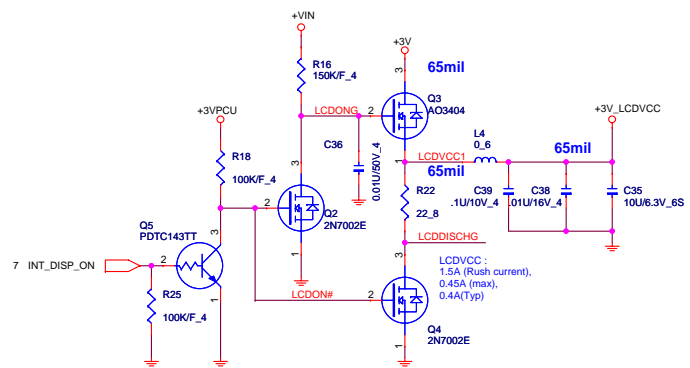
change C434 footprint to 0603



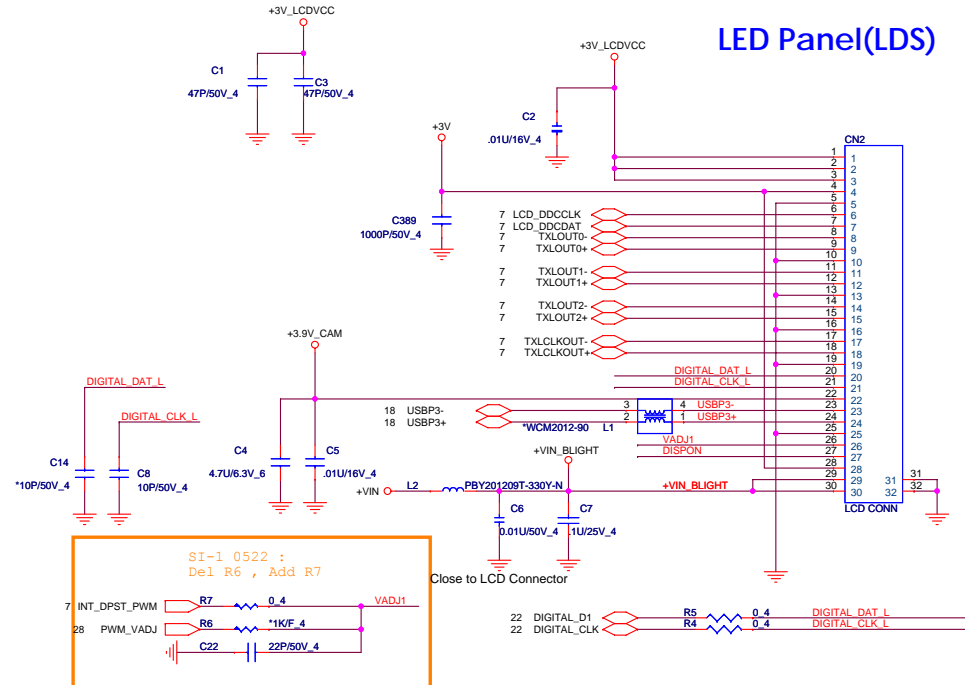
Backlight Control(LDS)



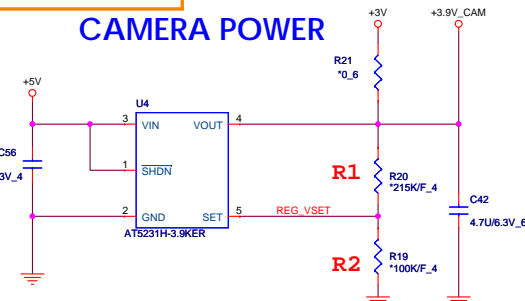
LCD POWER SWITCH



Request by HP RF(47Px2)



CAMERA POWER

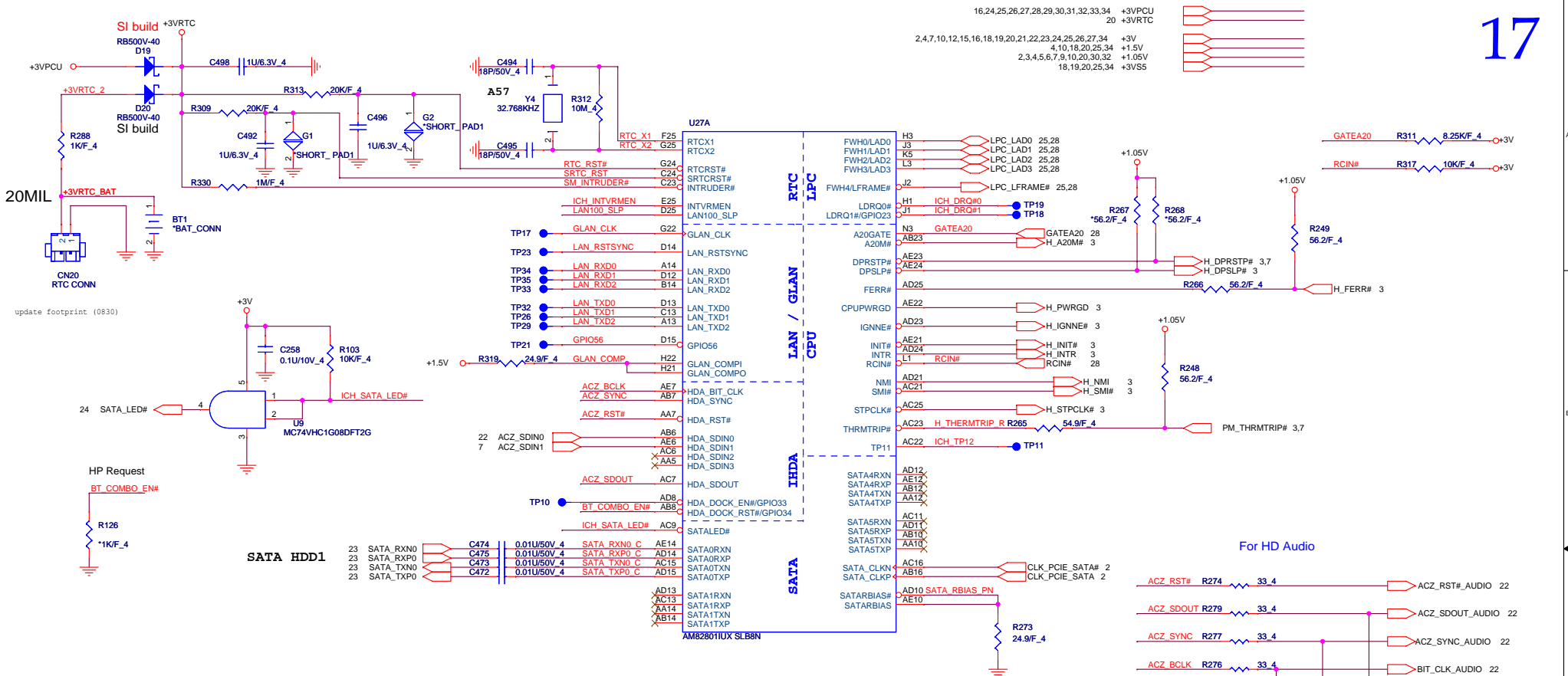


$$V_{out} = 1.25(1 + R1/R2)$$



PROJECT : FP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED Panel / Camera	1A
Date: Monday, May 25, 2009	Sheet 16 of 34	



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

Low = Internal VR disable
High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)

Low = Internal VR disable
High = Internal VR enable(Default)

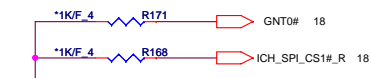
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPLCS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

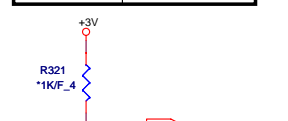


A16 swap override strap

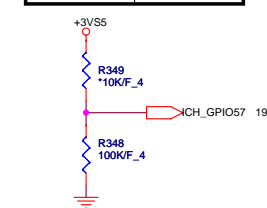
PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



No Reboot Strap	Low: Default Hi: No reboot
-----------------	-------------------------------



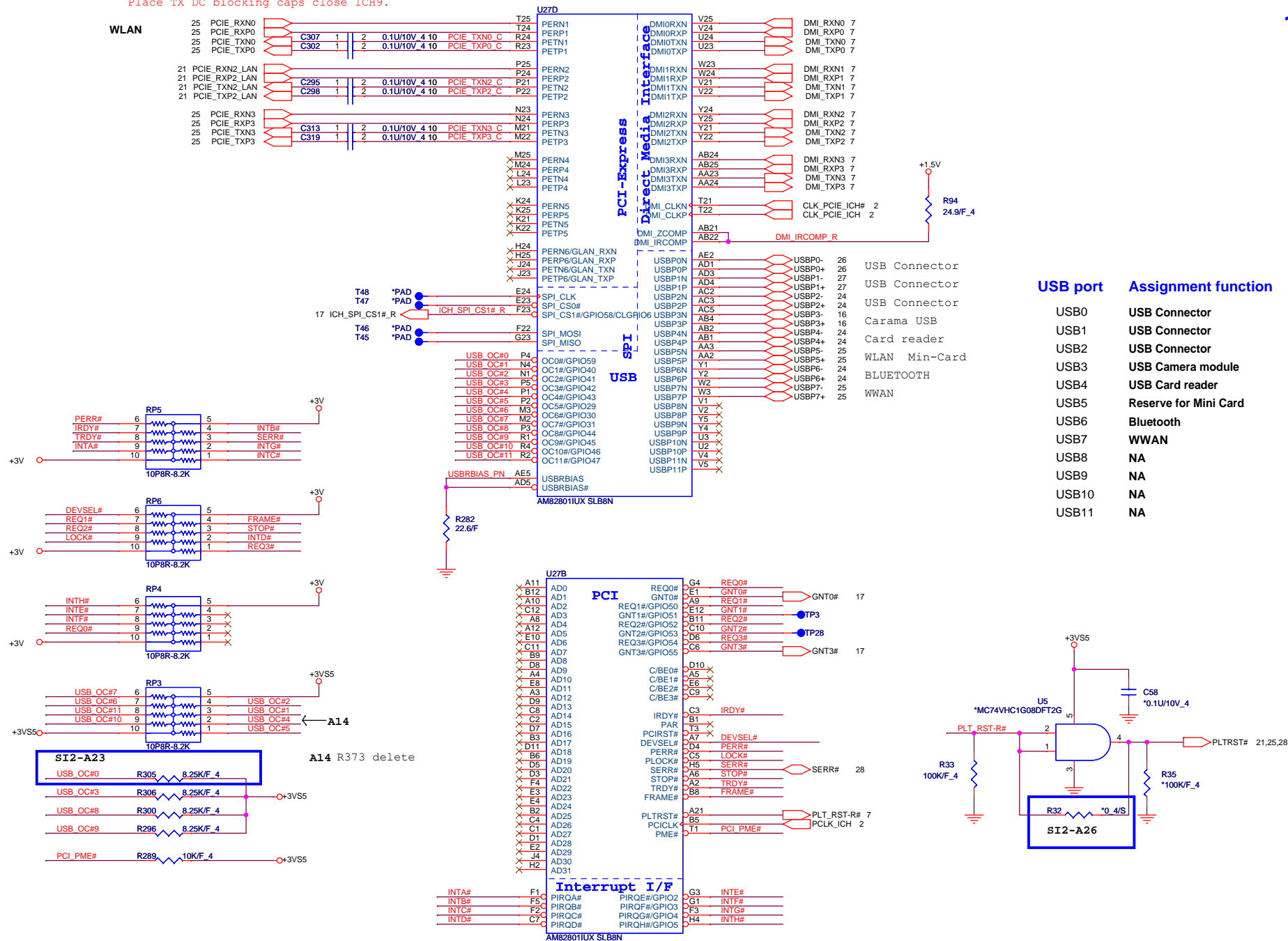
TPM physical presence	Low: Default
-----------------------	--------------



PROJECT : FP7
Quanta Computer Inc.

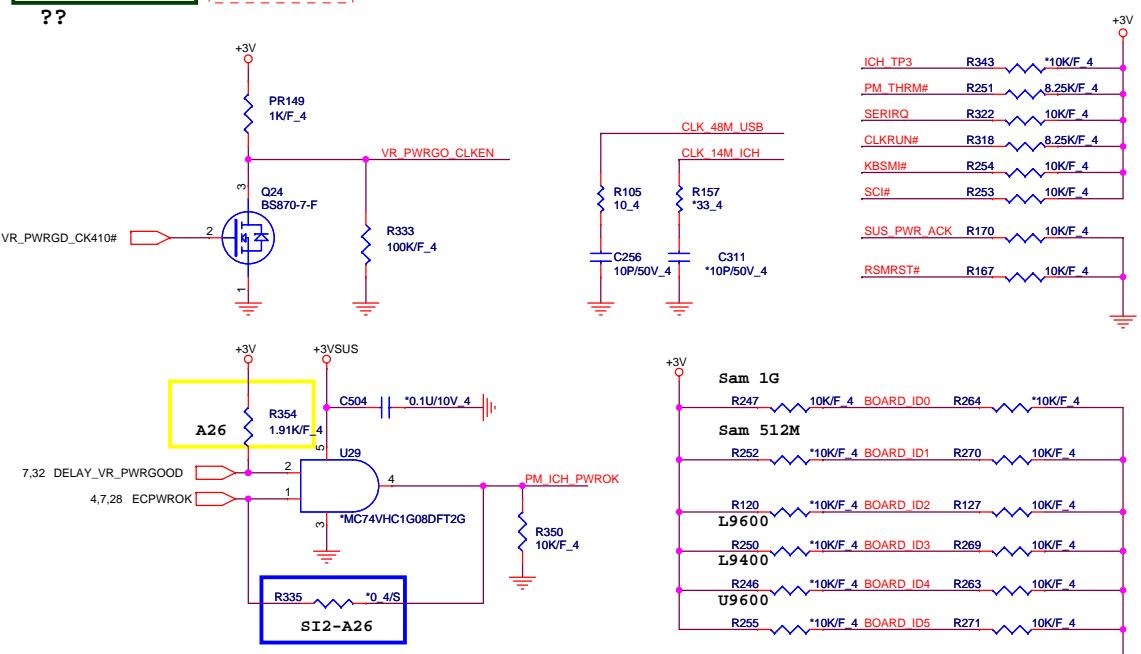
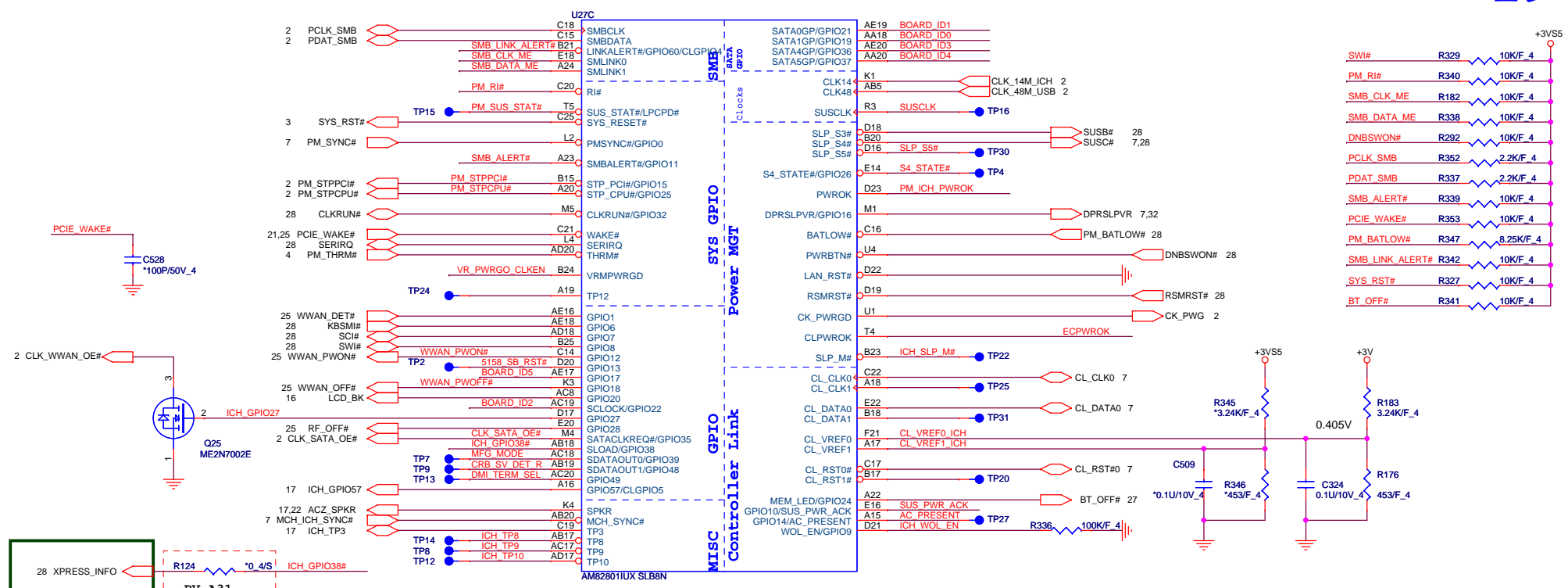
Size Custom	Document Number ICH9 (SATA/CPU)	Rev 1A
Date: Thursday, May 21, 2009	Sheet 17 of 34	

Place TX DC blocking caps close ICH9.



PROJECT : FP7
Quanta Computer Inc.

Size Custom Document Number ICH9 (USB/PCIE/DMI) Rev 1A
Date: Thursday, May 21, 2009 Sheet 18 of 34



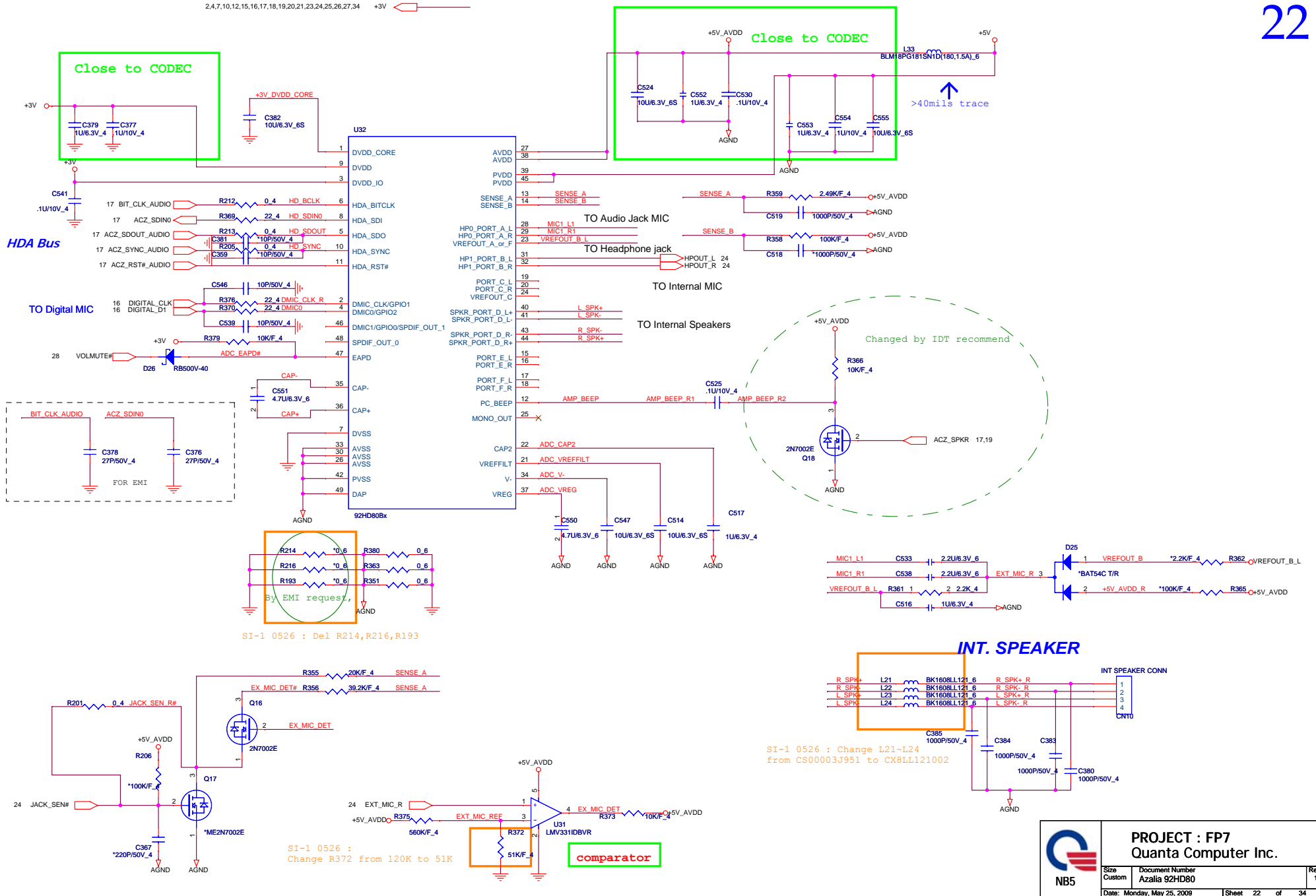
PV Update Board ID table

	Board ID 0 GPIO19	Board ID 1 GPIO21	Board ID 2 GPIO22	Board ID 3 GPIO36	Board ID 4 GPIO37	Board ID 5 GPIO17
RESERVE	0	0	0	0	0	0
Samsung IG	1	0	0	0	0	0
Samsung 512M	0	1	0	0	0	0
RESERVE	0	0	0	0	0	0
L9600 2.13G	1	0	0	1	0	0
L9400 1.86G	1	0	0	0	1	0
U9600 1.6G	1	0	0	0	0	1

Board ID 0
Board ID 1
Board ID 2
Board ID 3
Board ID 4
Board ID 5

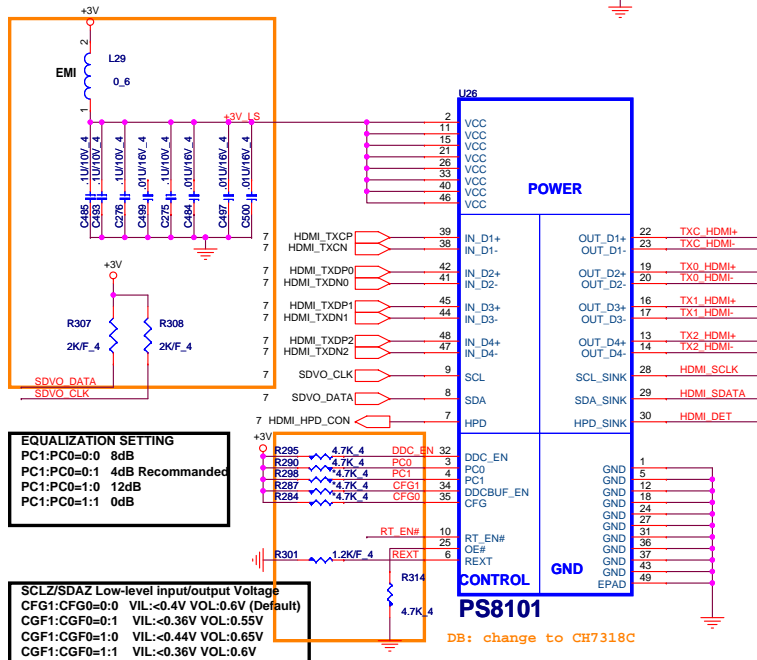


PROJECT : FP7
Quanta Computer Inc.



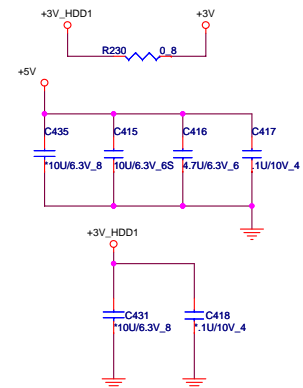
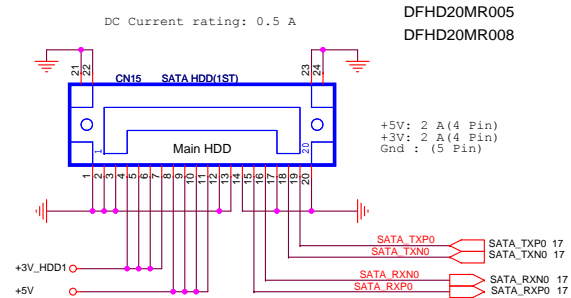
	PDT	CHR	NXP
R631	NC	0	0
R596	NC	4.7K	NC
R605	NC	4.7K	NC
R608	4.7K	4.7K	NC
R558	100K	NC	NC
R594	499	1.2K	10K
R550	7.5K	7.5K	7.5K
R552	20K	20K	20K
R595	NC	NC	NC
Q31	2N7002	NC	NC
R860	NC	4.7K	4.7K
R557	NC	100K	100K
D6	NC	NC	BAV99W

SI-1 0522 :
Add L29, C485, C493, C276,
C499, C275, C484, C497, C500, R307, R308

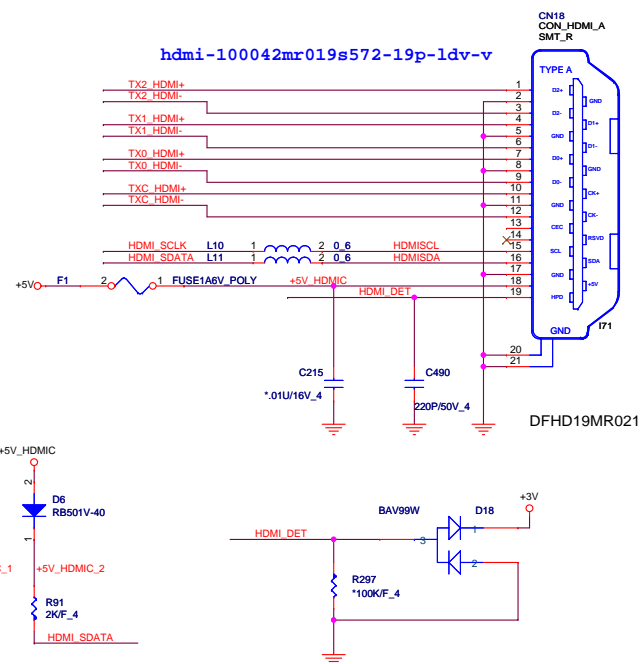


SI-1 0522 :
Add R295, R290, R301, R314
Change R301 from 499 to 1.2K

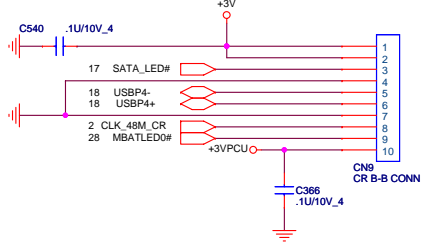
2.5" SATA HDD OR SSD(TOSHIBA)



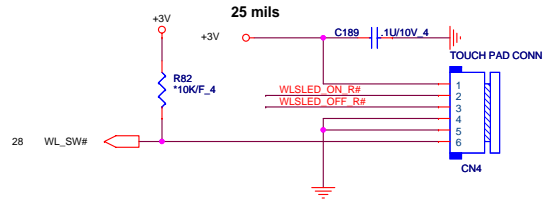
HDMI Connector



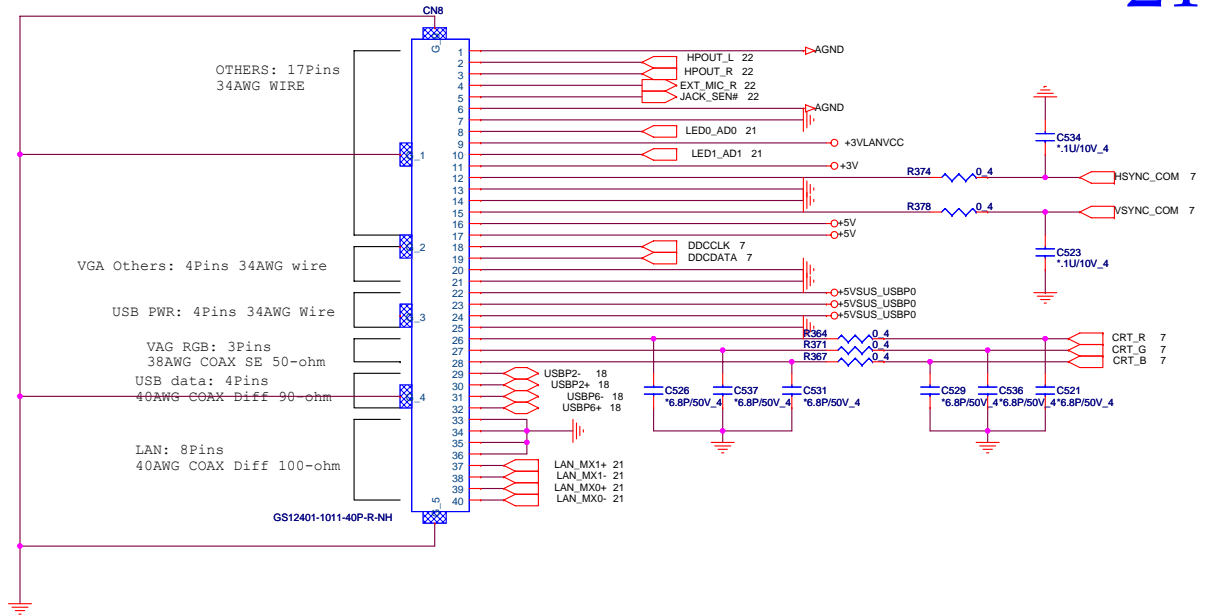
CardReader CONN.



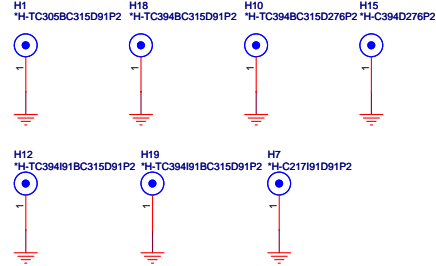
WL CTRL CONN.



I/O Board CONN.



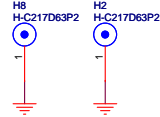
PCB Screws



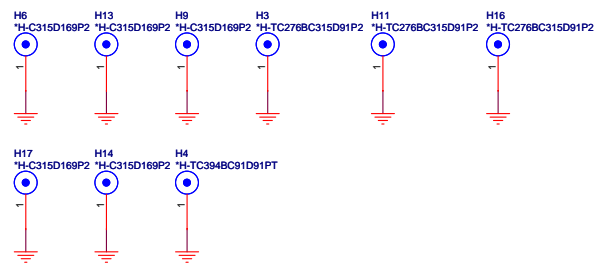
FAN Hole



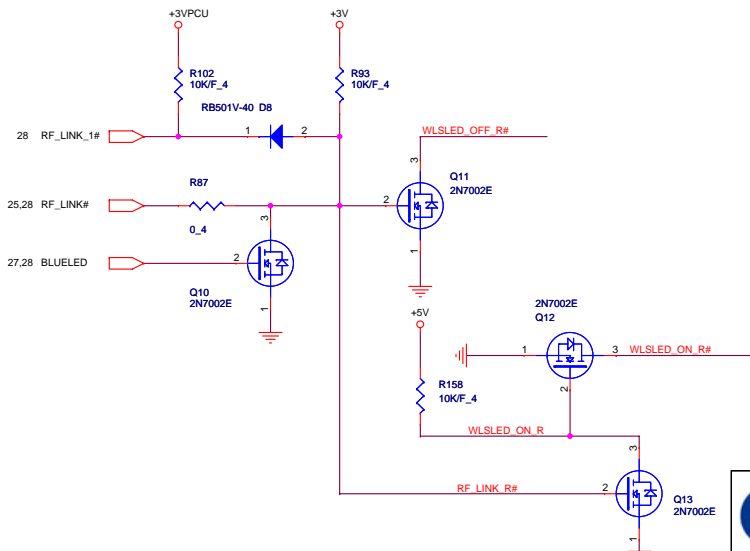
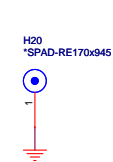
FAN SCREW HOLE



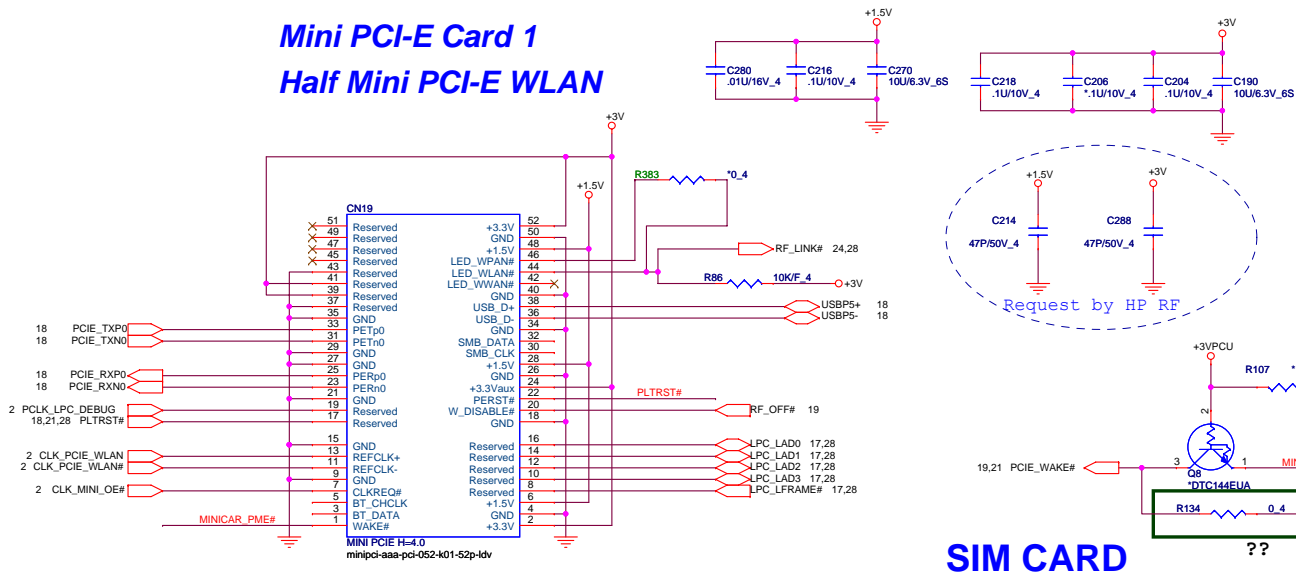
BRACKET



GND PAD



Mini PCI-E Card 1 Half Mini PCI-E WLAN

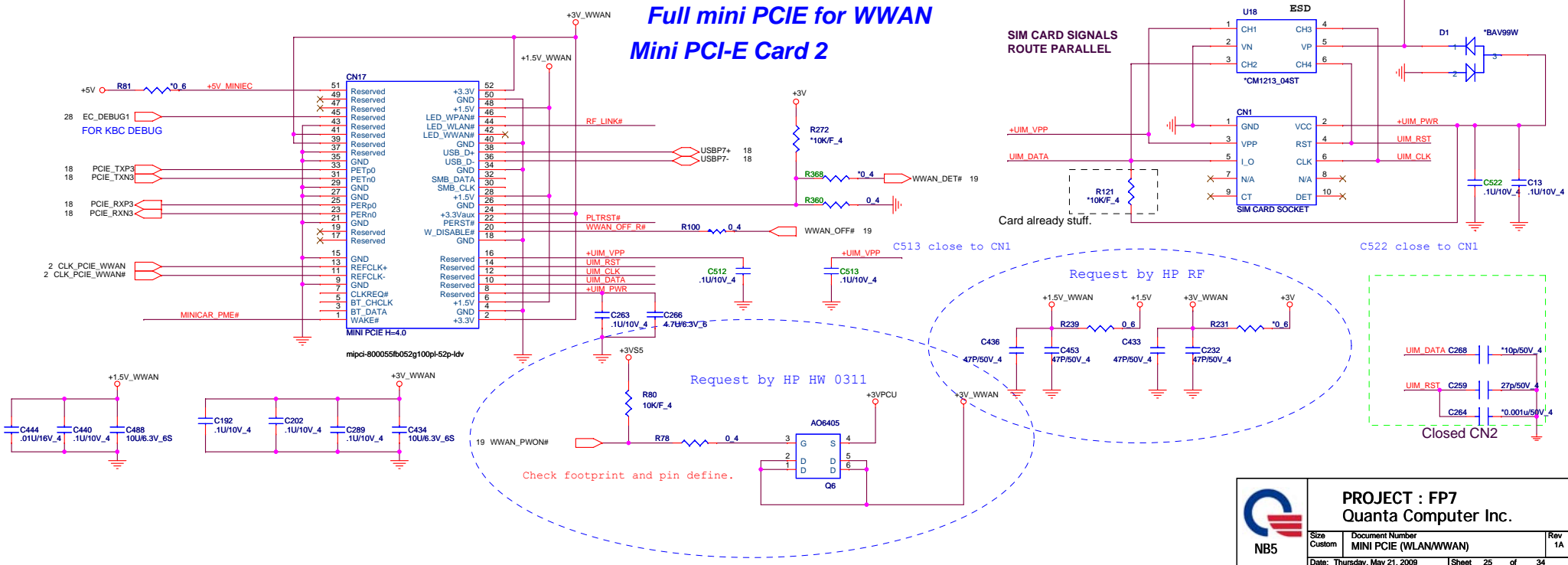


The value of the capacitor is suggest by Siemens HQ expert.
For against 300MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.

25

SIM CARD

Full mini PCIE for WWAN Mini PCI-E Card 2



SIM CARD SIGNALS
ROUTE PARALLEL

Card already stuff.

Request by HP RF

C513 close to CN1

C522 close to CN1

Request by HP HW 0311

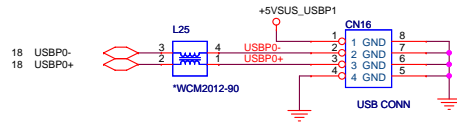
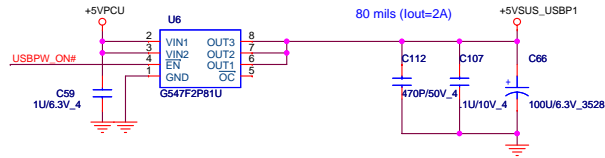
Check footprint and pin define.



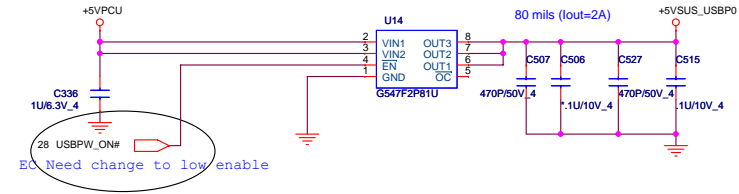
PROJECT : FP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE (WLAN/WWAN)	1A
Date: Thursday, May 21, 2009	Sheet 25 of 34	

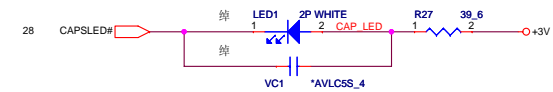
1x Left side USB PORT



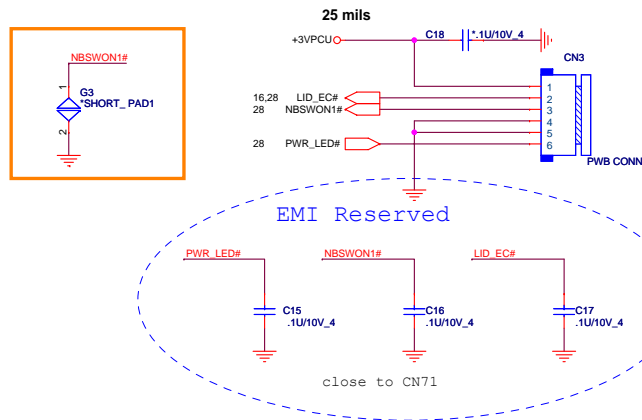
For Right 2xUSB Ports PWR



CAPS LEDs

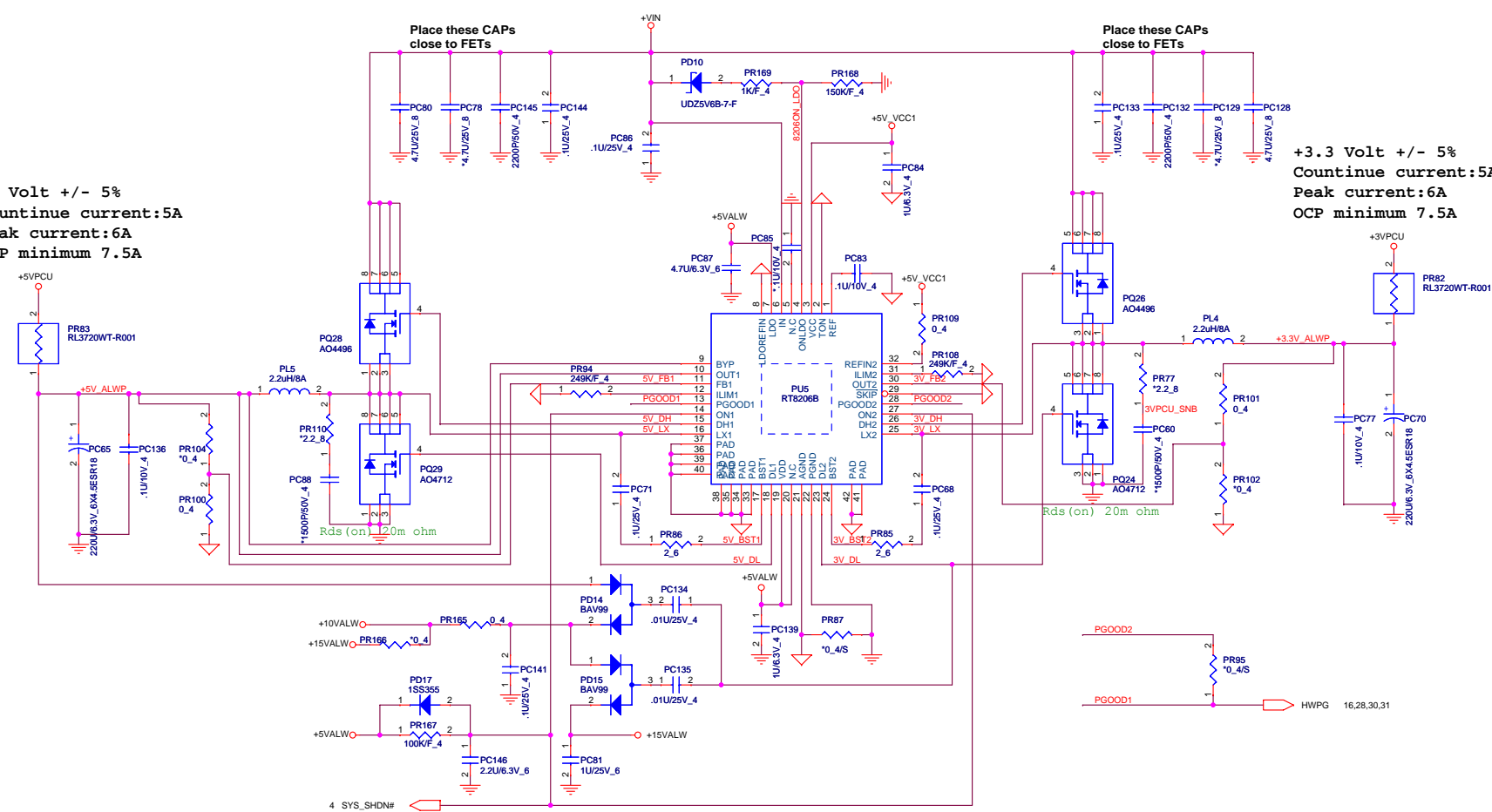


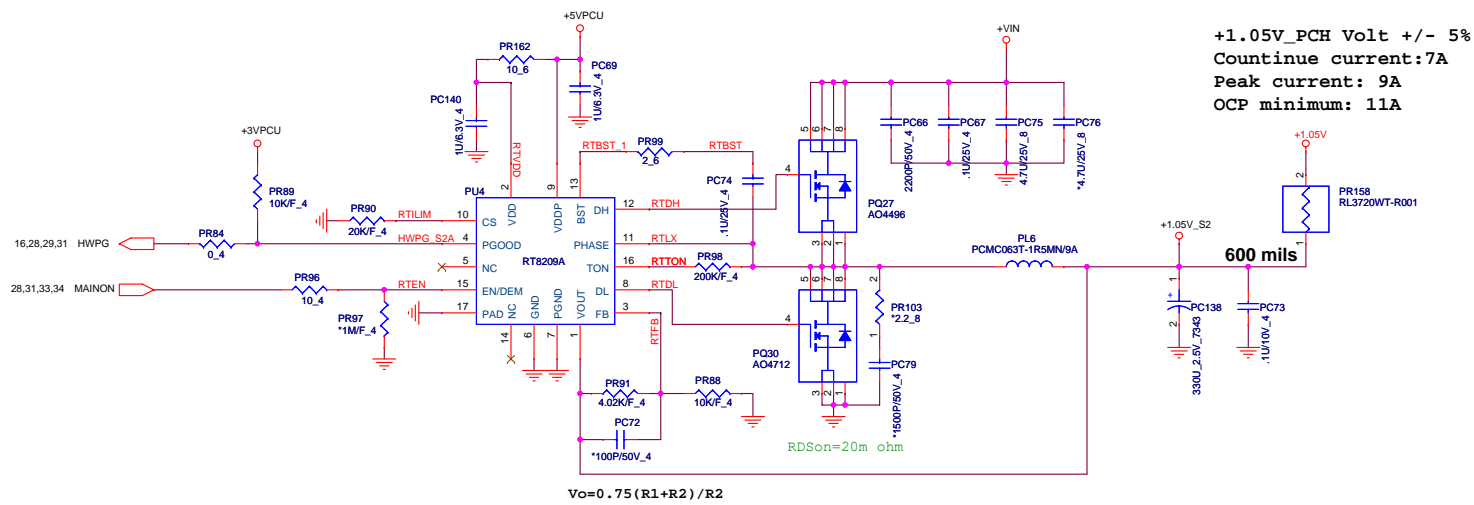
PWR BT CONN.



+5 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A

+3.3 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A





PROJECT : FP7 (CULV)
Quanta Computer Inc.

Size Custom	Document Number +1.1V VTT / PCH	Rev 1A
Date: Thursday, May 21, 2009	Sheet 30 of 34	

